EE 435
Lecture 14

Two-Stage Op Amp Design

- Architectures
- Compensation
  - First-stage compensation
  - Load compensated
  - Miller Compensation

Cascaded Amplifier Summary

$$A = \frac{A_0\,\tilde{p}}{s+\tilde{p}} \qquad \tilde{p}_2 = k\tilde{p}_1$$

- Single-stage amplifiers

  -- widely used in industry, little or no concern about compensation

- Two amplifier cascades – for separated poles $\quad 4\beta\,A_{0TOT} > k > 2\beta\,A_{0TOT}$

  -- widely used in industry but compensation is essential

  -- spread dependent upon β and most stringent for large β

- Three amplifier cascades - for ideally identical stages $\quad 8 > \beta A_0^3$

  -- seldom used in industry !

- Three amplifier cascades - for separated poles

$$(1+k_2+k_3)(k_2+k_3+k_2k_3) > \beta A_{0TOT}$$

  -- seldom used in industry but starting to appear but compensation essential!

- Four or more amplifier cascades - problems even larger than for three stages

  -- seldom used in industry !

Note: Some amplifiers that are termed single-stage amplifiers in many books and papers are actually two-stage amplifiers and some require modest compensation. Some that are termed two-stage amplifiers are actually three-stage amplifiers. These invariable have a very small gain on the first stage and a very large bandwidth. The nomenclature on this summary refers to the number of stages that have reasonably large gain.

Review from Last Time

Pole approximation methods

1. Consider all shunt capacitors

2. Decompose these into two sets, those that create low frequency poles and those that create high frequency poles (large capacitors create low frequency poles and small capacitors create high frequency poles)
   $\{C_{L1}, \ldots C_{Lk}\}$ and $\{C_{H1}, \ldots C_{Hm}\}$

3. To find the k low frequency poles, replace all independent voltage sources with ss shorts and all independent current sources with ss opens, all high-frequency capacitors with ss open circuits and, one at a time, select C_{Lh} and determine the impedance facing it, say R_{Lh} if all other low-frequency capacitors are replaced with ss short circuits. Then an approximation for the pole corresponding to C_{Lh} is

$$p_{Lh}=-1/(R_{Lh}C_{Lh})$$

4. To find the m high-frequency poles, replace all independent voltage sources with ss shorts and all independent current sources with ss opens, replace all low-frequency capacitors with ss short circuits and, one at a time, select C_{Hh} and determine the impedance facing it, say R_{Hh} if all other high-frequency capacitors are replaced with ss open circuits. Then the approximation for the pole corresponding to C_{Hh} is

$$p_{Hh}=-1/(R_{Hh}C_{Hh})$$

Compensation of Two-Stage Cascade

Definition

- "Compensation" is the modification of the op amp frequency response (that of the open-loop amplifier) so that acceptable ringing or overshoot or lack thereof in the closed-loop response is achieved

- Often do compensation for feedback amplifier applications though could compensate for closed-loop performance in other applications such as in a filter

- If two stages in cascade are first-order lowpass, compensation strategy is often to make an adequate pole spread to get acceptable closed-loop performance

- Often focus on the poles on the two nodes if cascade is of first-order lowpass stages

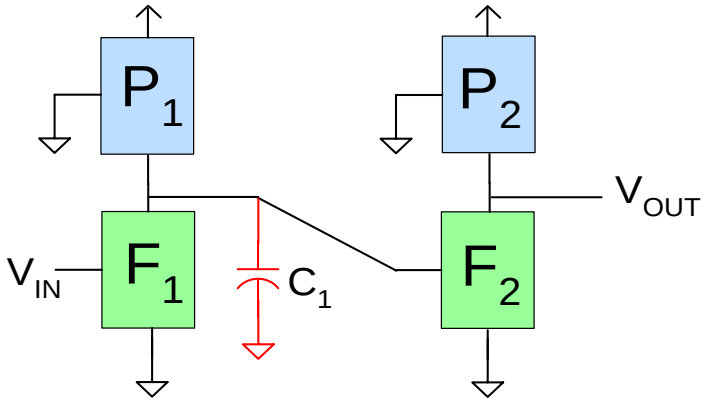
- If large spread of two poles that may inherently be close is required, can make one much larger or make one much smaller but fundamental speed limitations in a process often make it impossible to make one pole much larger so only alternative is often to make one pole much smaller

Note: Have intentionally not mentioned the term "stability" when discussing compensation

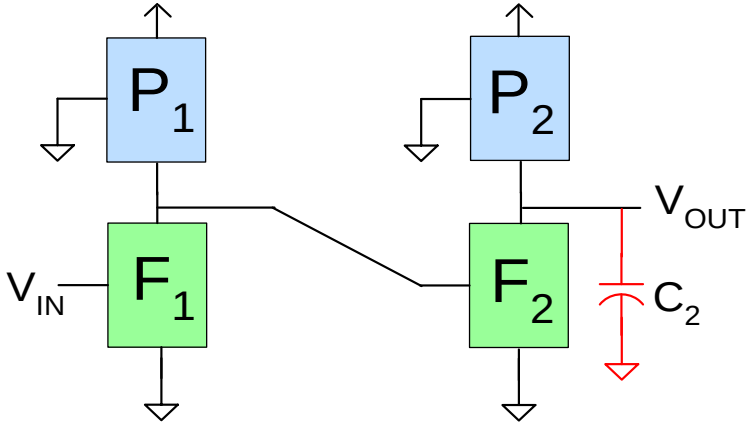
Review from Last Time

Compensation of Basic Two-Stage Cascade

(shown for single input, single output but applicable to differential as well)



Internal Node Compensated



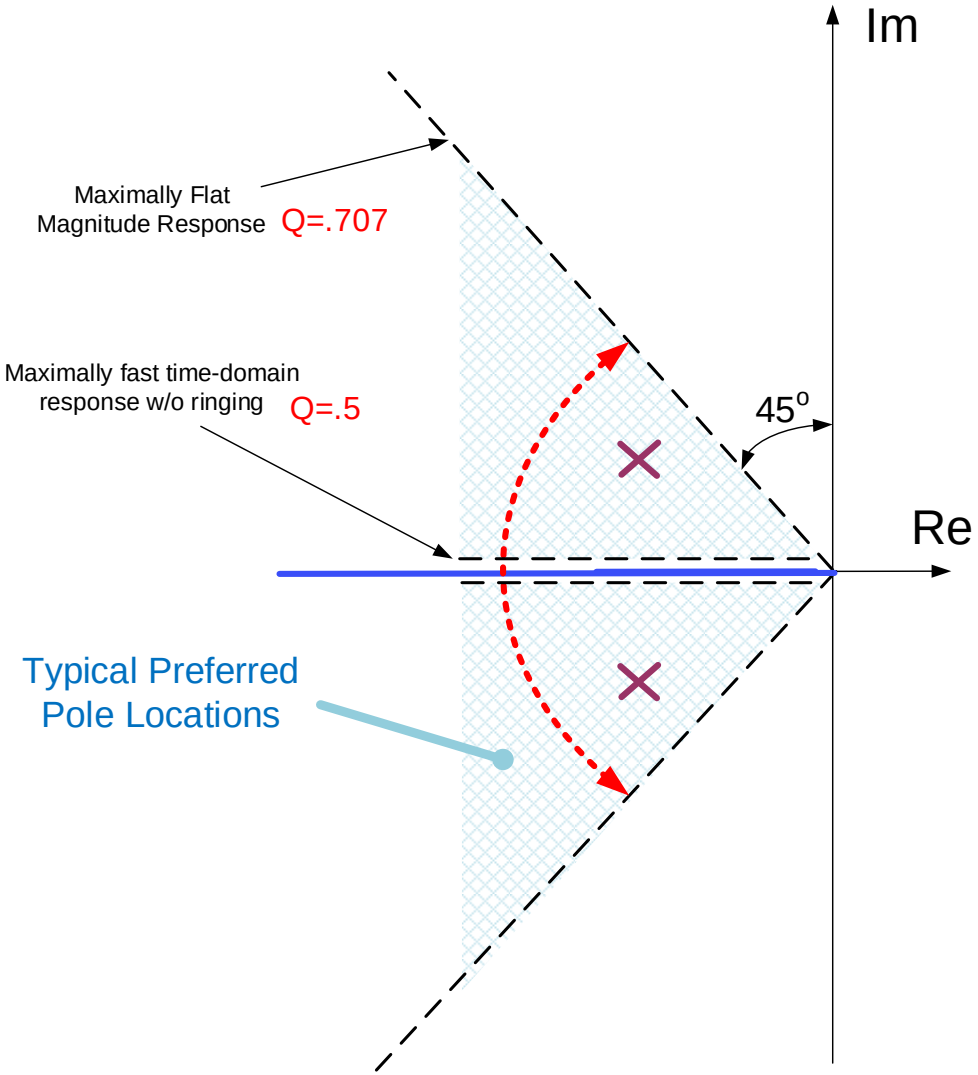
Output Compensated

- Modest variants of the compensation principle are often used
- Internal Node compensated creates the dominant pole on the internal node
- Output compensated creates the dominant pole on the external node
- Output compensated often termed “self-compensated”
- Internally Compensated denotes Internal Node compensation with compensation circuit on-chip

Everything else is just details !!

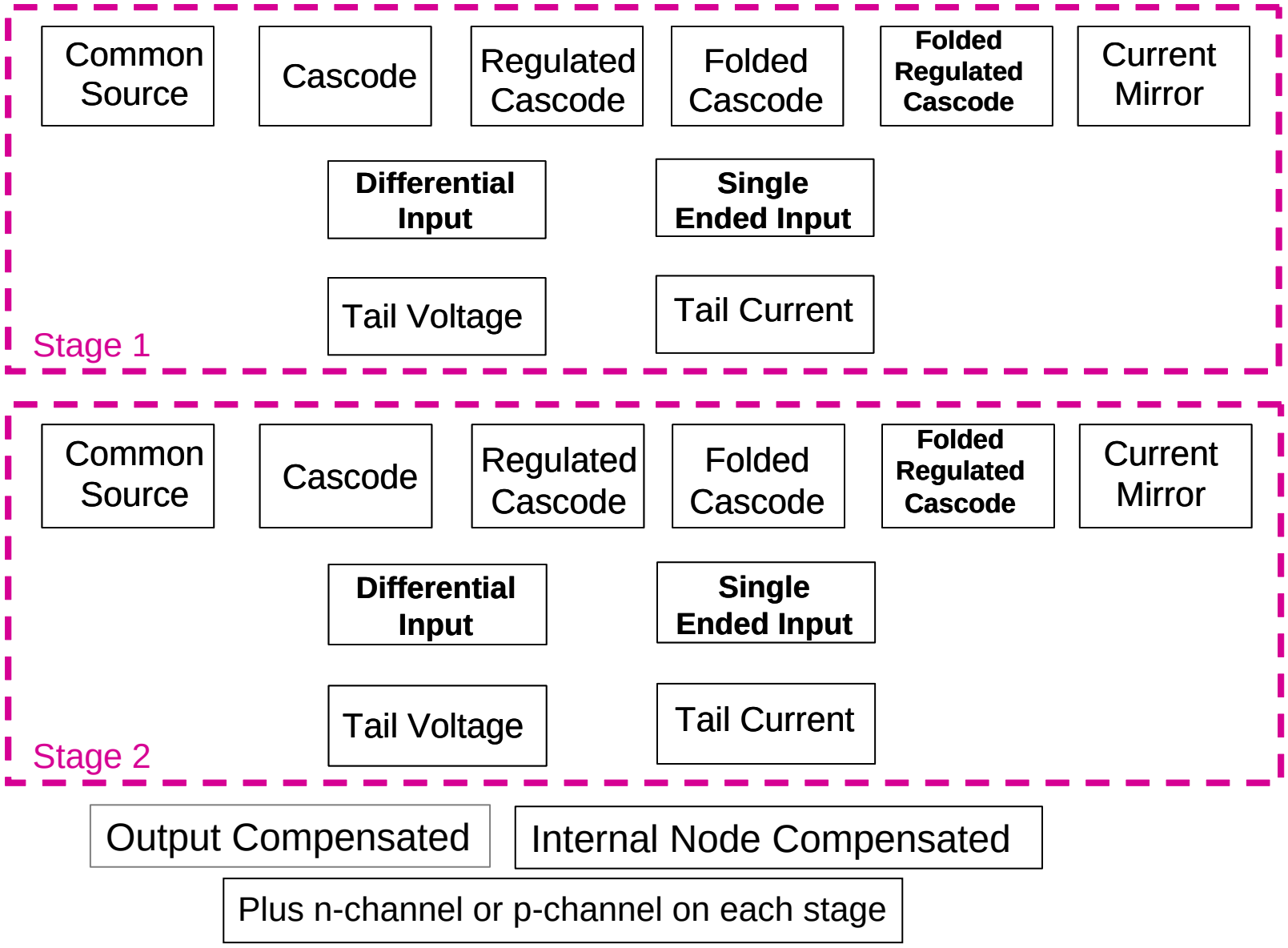
Common Compensation Goal

Typical Target Closed-loop Pole Locations for Feedback Amplifiers



Review from Last Time

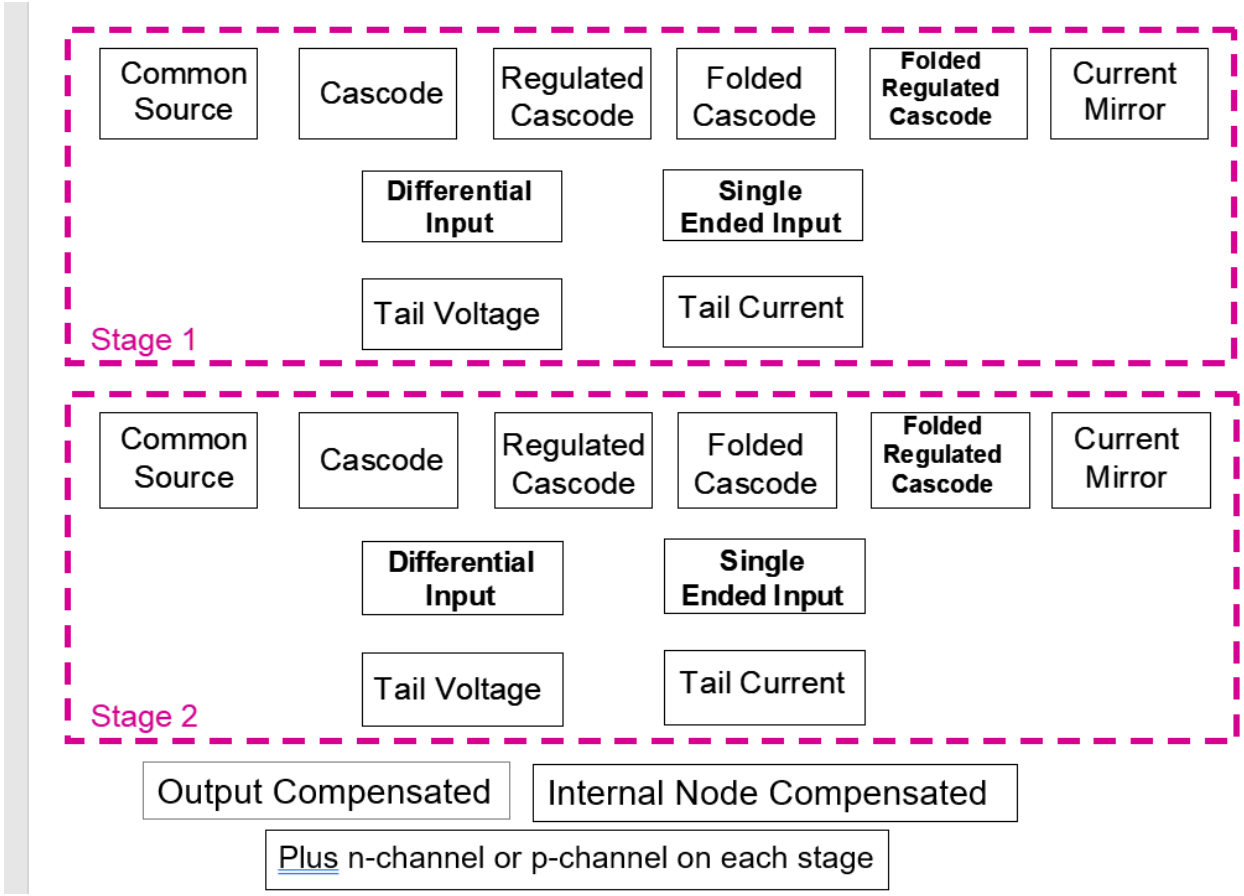
Two-stage Architectural Choices



4608 Choices !!!

Review from Last Time

Two-stage Architectural Choices



Which of these 4608 choices can be used to build a good op amp?

All of them !!

Two-stage Architectural Choices

There are actually a few additional variants so the number of choices is larger

Basic analysis of all is about the same and can be obtained from the quarter circuit of each stage

A very small number of these are actually used

Some rules can be established that provide guidance as to which structure may be most useful in a given application

Two-stage Architectural Choices

Guidelines for Architectural Choices

Tail current source usually used in first stage, tail voltage source in second stage

Large gain usually used in first stage, smaller gain in second stage

First and second stage usually use quarter circuits of opposite types (n-p or p-n)

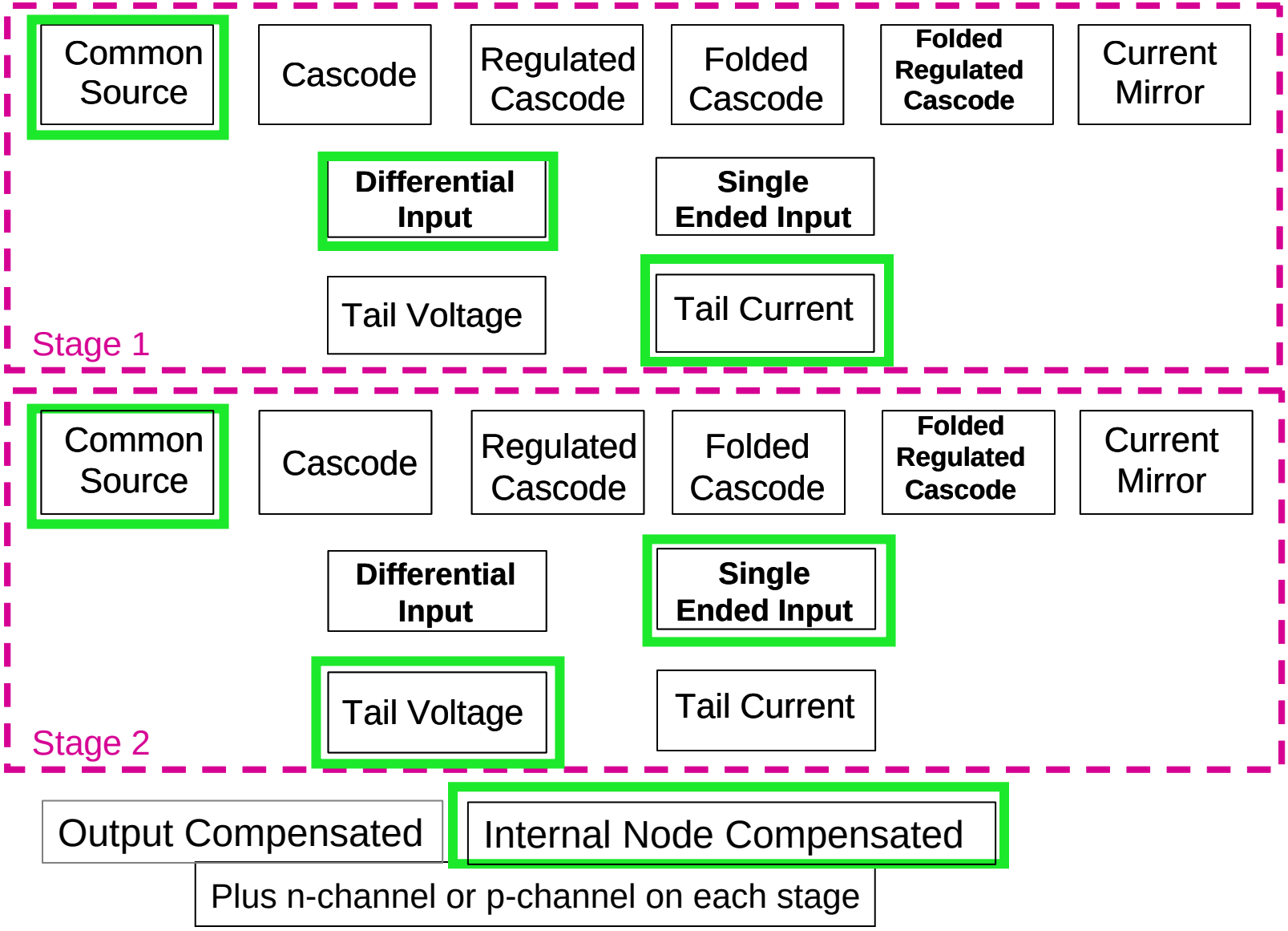
Common mode input range of concern on first stage but output swing of first stage of reduced concern. Output range on second stage of concern.

CMRR of first stage of concern but not of second stage

Noise on first stage of concern but not of much concern on second stage

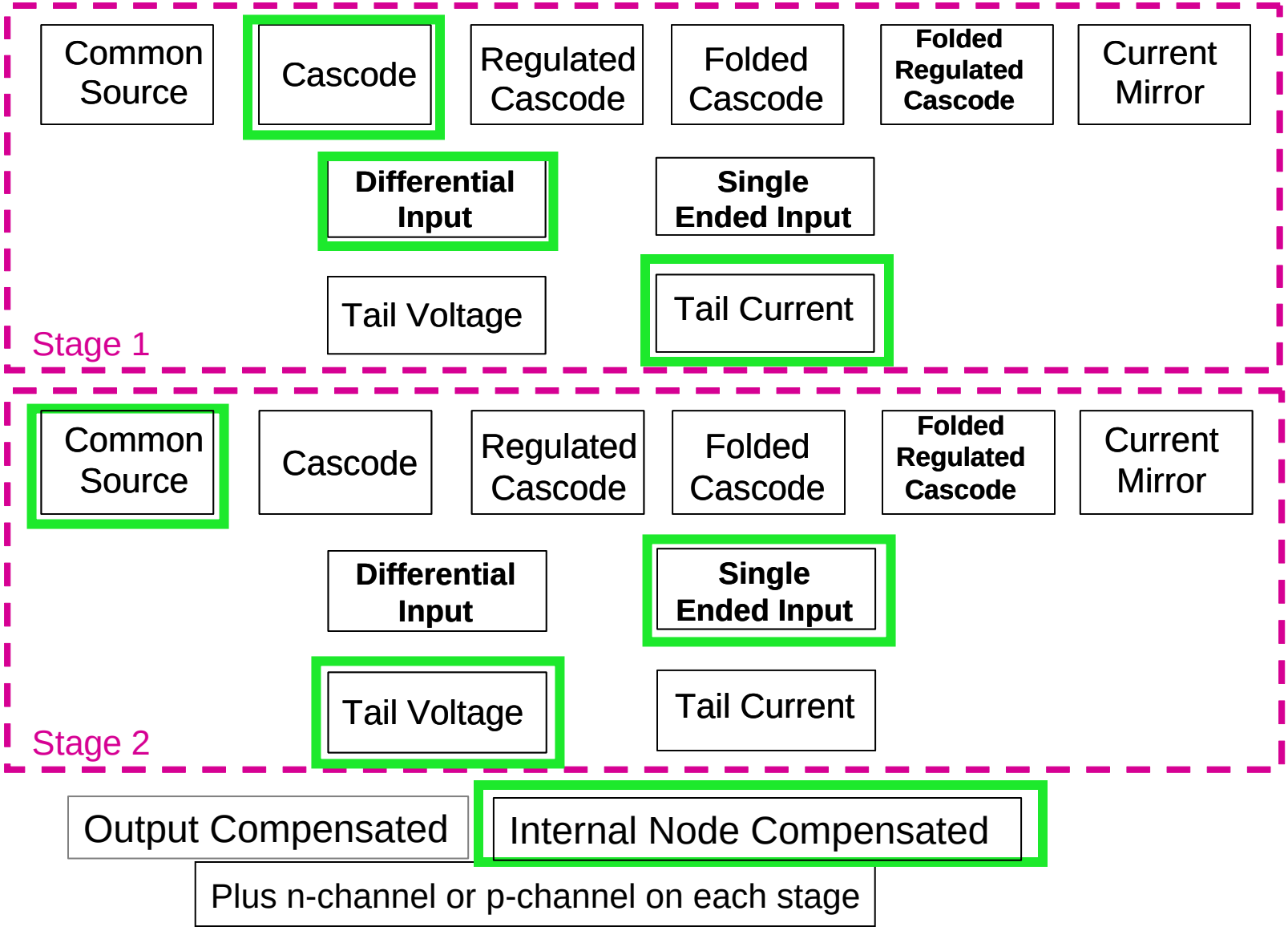
Offset voltage usually dominated by that of the first stage

Two-stage Architectural Choices



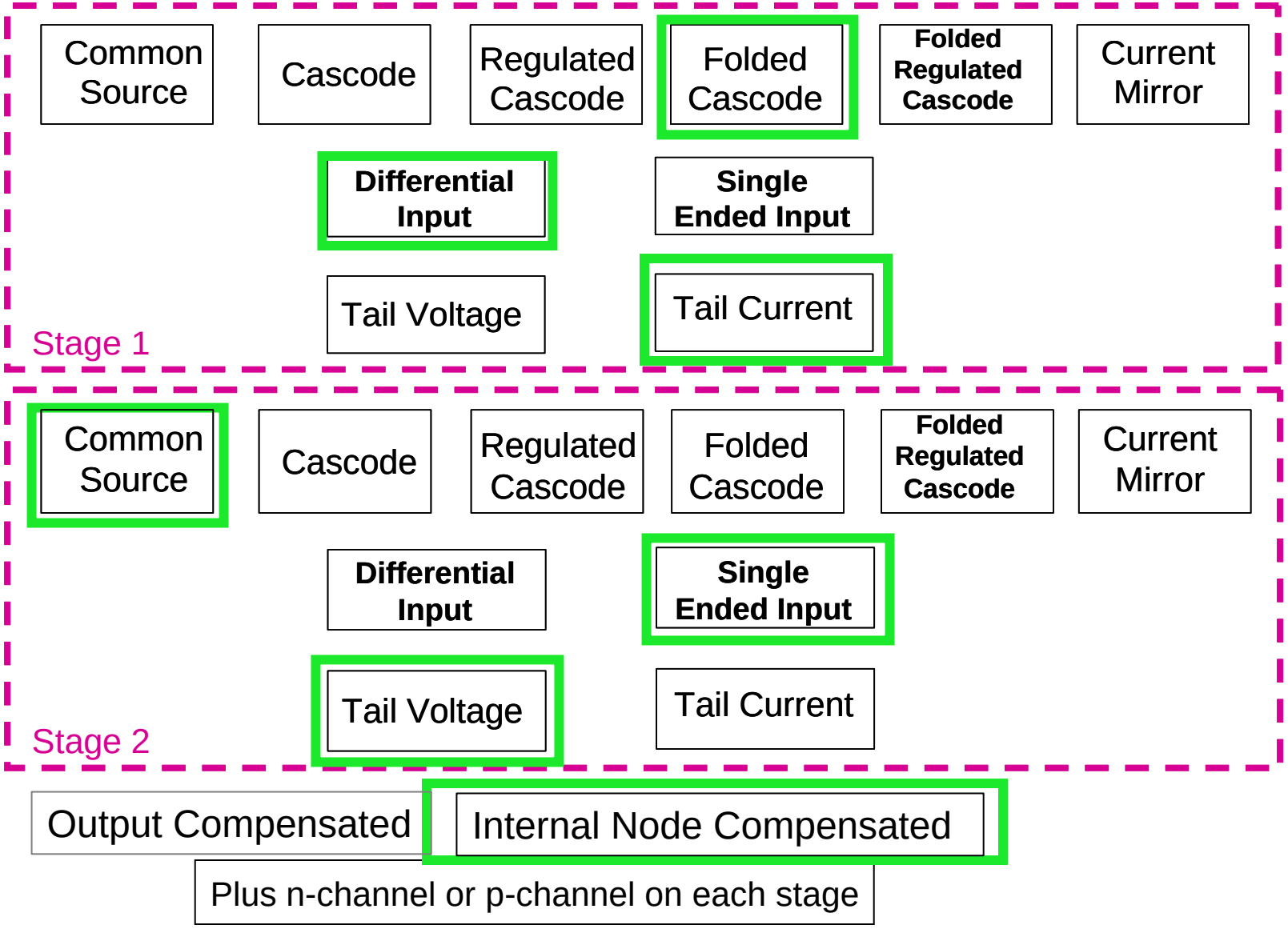
Basic Two-Stage Op Amp

Two-stage Architectural Choices



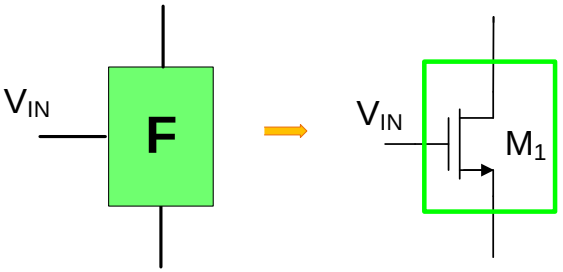
Cascode-Cascade Two-Stage Op Amp

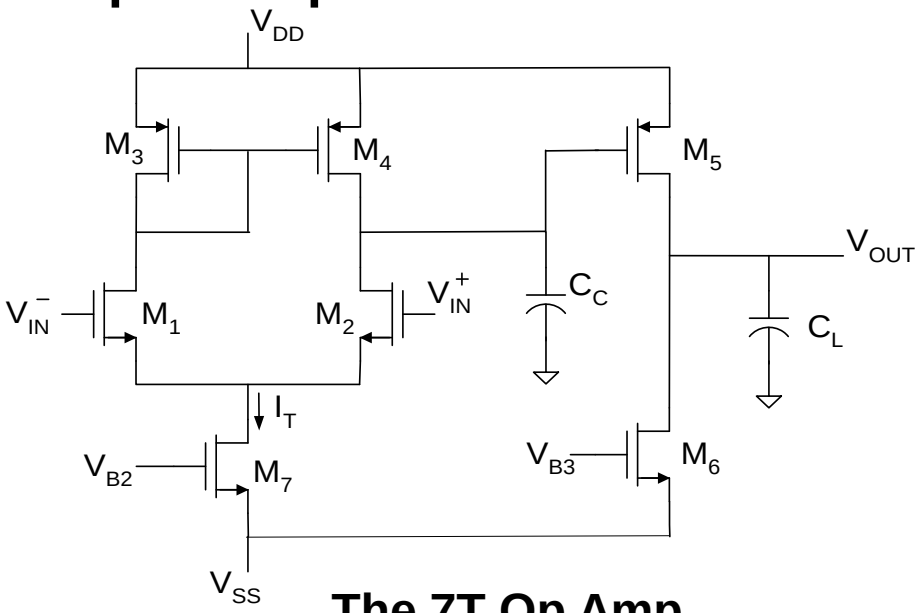
Two-stage Architectural Choices



Folded Cascode-Cascade Two-Stage Op Amp

Basic Two-Stage Op Amp (compensated on first stage)





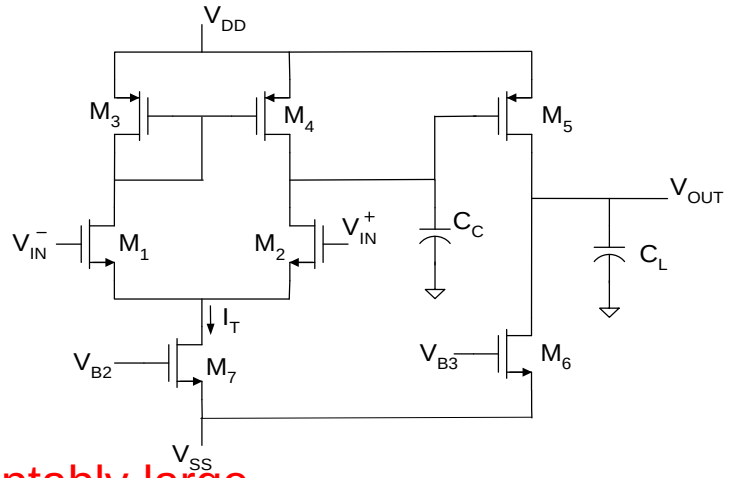
The 7T Op Amp

- dc gain is product of first stage and second stage gains: $A=A_{01}A_{02}$
- One of the most widely used op amp architectures
- Essentially just a cascade of two common-source stages
- Compensation Capacitor C_C used to get wide pole separation
- Pole on drain node of M_1 usually of little concern
- Two poles in differential operation of amplifier usually dominate performance
- C_C can be internal (termed internally compensated) or external (termed externally compensated)
- External compensation works but is usually not practical
- No universally accepted strategy for designing this seemingly simple amplifier

Pole spread $2\beta A_{01}A_{02} < k < 4\beta A_{01}A_{02}$ makes C_C unacceptably large for on-chip solutions

Basic Two-Stage Op Amp

The 7T Op Amp



Pole spread $\propto \beta A_{01} A_{02}$ makes C_C unacceptably large

- Remember, pole spread strongly dependent upon β
- Large β (i.e. β=1) requires large C_C
- C_C is usually an additional capacitor that is added
- Concept of Miller compensation will be used to reduce actual size of C_C

What about just making C_C larger than what is needed?

GB will degrade, power and area will increase

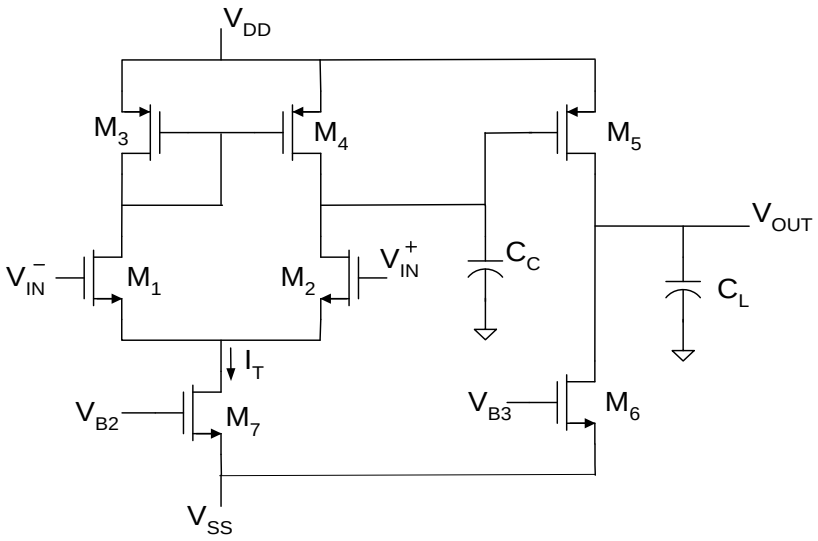
What about providing additional compensation by making C_L larger too?

Poles will move together and degrade performance

What about compensating for worst-case β=1 so β dependence can be ignored?

- Good solution for catalog parts so application space large but at a cost !
- Penalty in GB, power, and area sever if compensated for much different β than needed

Basic Two-Stage Op Amp



Pole spread $\propto \beta A_{01} A_{02}$ makes C_C unacceptably large

Important to compensate just for what is needed, even a little more comes at a rather big penalty in performance, power, or area !!

Selected Commercial Op Amps

TEXAS INSTRUMENTS

www.ti.com

SNOSBH1D – MAY 1999 – REVISED MARCH 2013

LF147/LF347 Wide Bandwidth Quad JFET Input Operational Amplifiers

Check for Samples: LF147, LF347-N

FEATURES

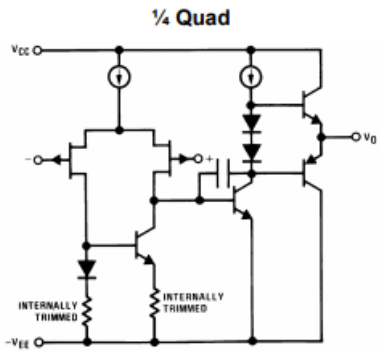
- Internally Trimmed Offset Voltage: 5 mV max
- Low Input Bias Current: 50 pA
- Low Input Noise Current: 0.01 pA/√Hz
- Wide Gain Bandwidth: 4 MHz
- High Slew Rate: 13 V/μs
- Low Supply Current: 7.2 mA
- High Input Impedance: $10^{12}\Omega$
- Low Total Harmonic Distortion: ≤0.02%
- Low 1/f Noise Corner: 50 Hz
- Fast Settling Time to 0.01%: 2 μs

DESCRIPTION

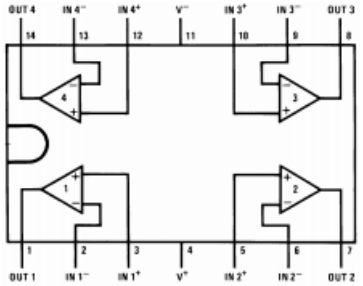
The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Simplified Schematic



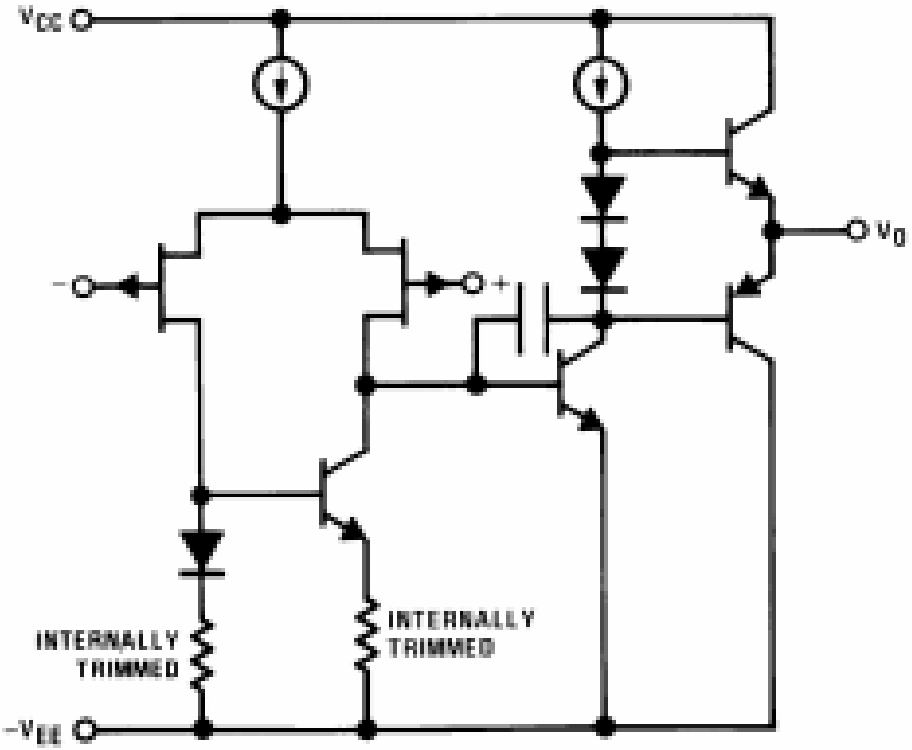
Connection Diagram



LF147 available as per JM38510/11906.

Figure 1. 14-Pin PDIP / CDIP / SOIC

Selected Commercial Op Amps



Selected Commercial Op Amps

TEXAS INSTRUMENTS

LM224K, LM224KA, LM324, LM324A, LM324K, LM324KA, LM2902
LM124, LM124A, LM224, LM224A, LM2902V, LM2902K, LM2902KV, LM2902KAV

SLOS066W – SEPTEMBER 1975 – REVISED MARCH 2015

LMx24, LMx24x, LMx24xx, LM2902, LM2902x, LM2902xx, LM2902xxx Quadruple Operational Amplifiers

1 Features

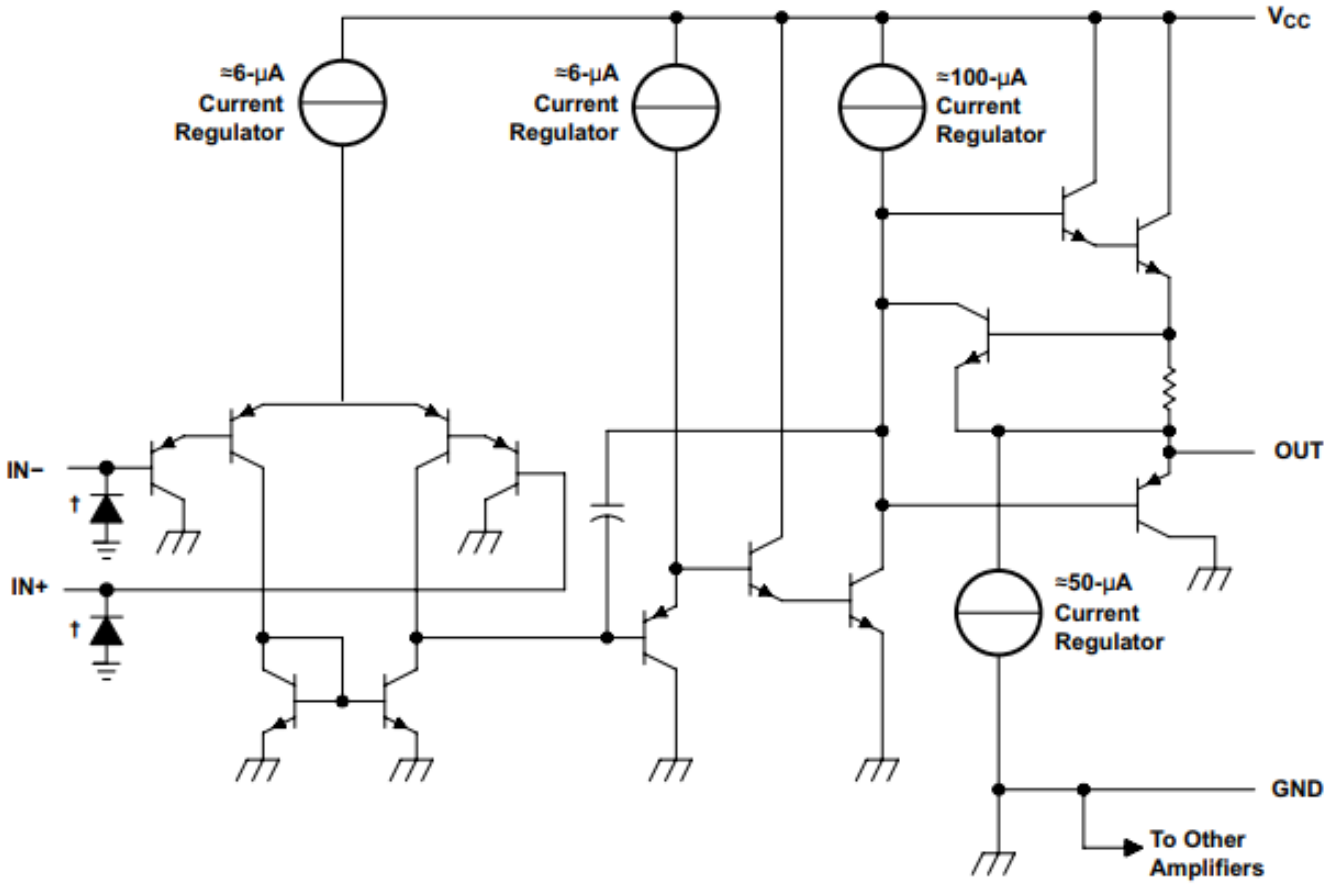
- 2-kV ESD Protection for:
  - LM224K, LM224KA
  - LM324K, LM324KA
  - LM2902K, LM2902KV, LM2902KAV
- Wide Supply Ranges
  - Single Supply: 3 V to 32 V (26 V for LM2902)
  - Dual Supplies: ±1.5 V to ±16 V (±13 V for LM2902)
- Low Supply-Current Drain Independent of Supply Voltage: 0.8 mA Typical
- Common-Mode Input Voltage Range Includes Ground, Allowing Direct Sensing Near Ground
- Low Input Bias and Offset Parameters
  - Input Offset Voltage: 3 mV Typical

2 Applications

- Blu-ray Players and Home Theaters
- Chemical and Gas Sensors
- DVD Recorders and Players
- Digital Multimeter: Bench and Systems
- Digital Multimeter: Handhelds
- Field Transmitter: Temperature Sensors
- Motor Control: AC Induction, Brushed DC, Brushless DC, High-Voltage, Low-Voltage, Permanent Magnet, and Stepper Motor
- Oscilloscopes
- TV: LCD and Digital
- Temperature Sensors or Controllers Using Modbus
- Weigh Scales

Selected Commercial Op Amps

8.2 Functional Block Diagram



Voltage Feedback Op Amp Gain and Bandwidth

INTRODUCTION

This tutorial examines the common ways to specify op amp gain and bandwidth. It should be noted that this discussion applies to voltage feedback (VFB) op amps—current feedback (CFB) op amps are discussed in a later tutorial (MT-034).

OPEN-LOOP GAIN

Unlike the ideal op amp, a practical op amp has a finite gain. The open-loop dc gain (usually referred to as A_{VOL}) is the gain of the amplifier without the feedback loop being closed, hence the name "open-loop." For a precision op amp this gain can be vary high, on the order of 160 dB (100 million) or more. This gain is flat from dc to what is referred to as the *dominant pole corner frequency*. From there the gain falls off at 6 dB/octave (20 dB/decade). An octave is a doubling in frequency and a decade is ×10 in frequency). If the op amp has a single pole, the open-loop gain will continue to fall at this rate as shown in Figure 1A. A practical op amp will have more than one pole as shown in Figure 1B. The second pole will double the rate at which the open-loop gain falls to 12 dB/octave (40 dB/decade). If the open-loop gain has dropped below 0 dB (unity gain) before it reaches the frequency of the second pole, the op amp will be unconditionally stable at any gain. This will be typically referred to as *unity gain stable* on the data sheet. If the second pole is reached while the closed-loop gain is greater than 1 (0 db), then the amplifier may not be stable. Some op amps are designed to be stable only at higher closed-loop gains, and these are referred to as *decompensated* op amps.

Selected Commercial Op Amps

Decompensated Op Amp

ANALOG DEVICES

30 V, High Speed, Low Noise, Low Bias Current, JFET Operational Amplifier

Data Sheet **ADA4627-1/ADA4637-1**

FEATURES

- Low offset voltage: 200 µV maximum
- Offset drift: 1 µV/°C typical
- Very low input bias current: 5 pA maximum
- Extended temperature range: −40°C to +125°C
- ±5 V to ±15 V dual supply
- ADA4627-1 GBW: 19 MHz
- ADA4637-1 GBW: 79 MHz
- Voltage noise: 6.1 nV/√Hz at 1 kHz
- ADA4627-1 slew rate: 82 V/µs
- ADA4637-1 slew rate: 170 V/µs
- High gain: 120 dB typical
- High CMRR: 116 dB typical
- High PSRR: 112 dB typical

APPLICATIONS

- High impedance sensors
- Photodiode amplifier
- Precision instrumentation
- Phase-locked loop filters
- High end, professional audio
- DAC output amplifier
- ATE
- Medical

PIN CONFIGURATIONS

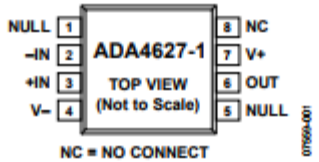


Figure 1. 8-Lead SOIC_N (R-8)

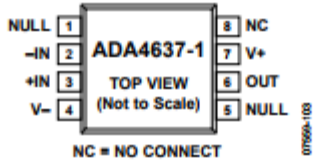


Figure 2. 8-Lead SOIC_N (R-8)

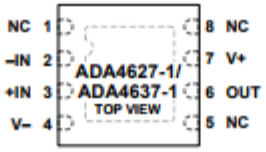


Figure 3. 8-Lead LFCSP_VD (CP-8-13)

Selected Commercial Op Amps

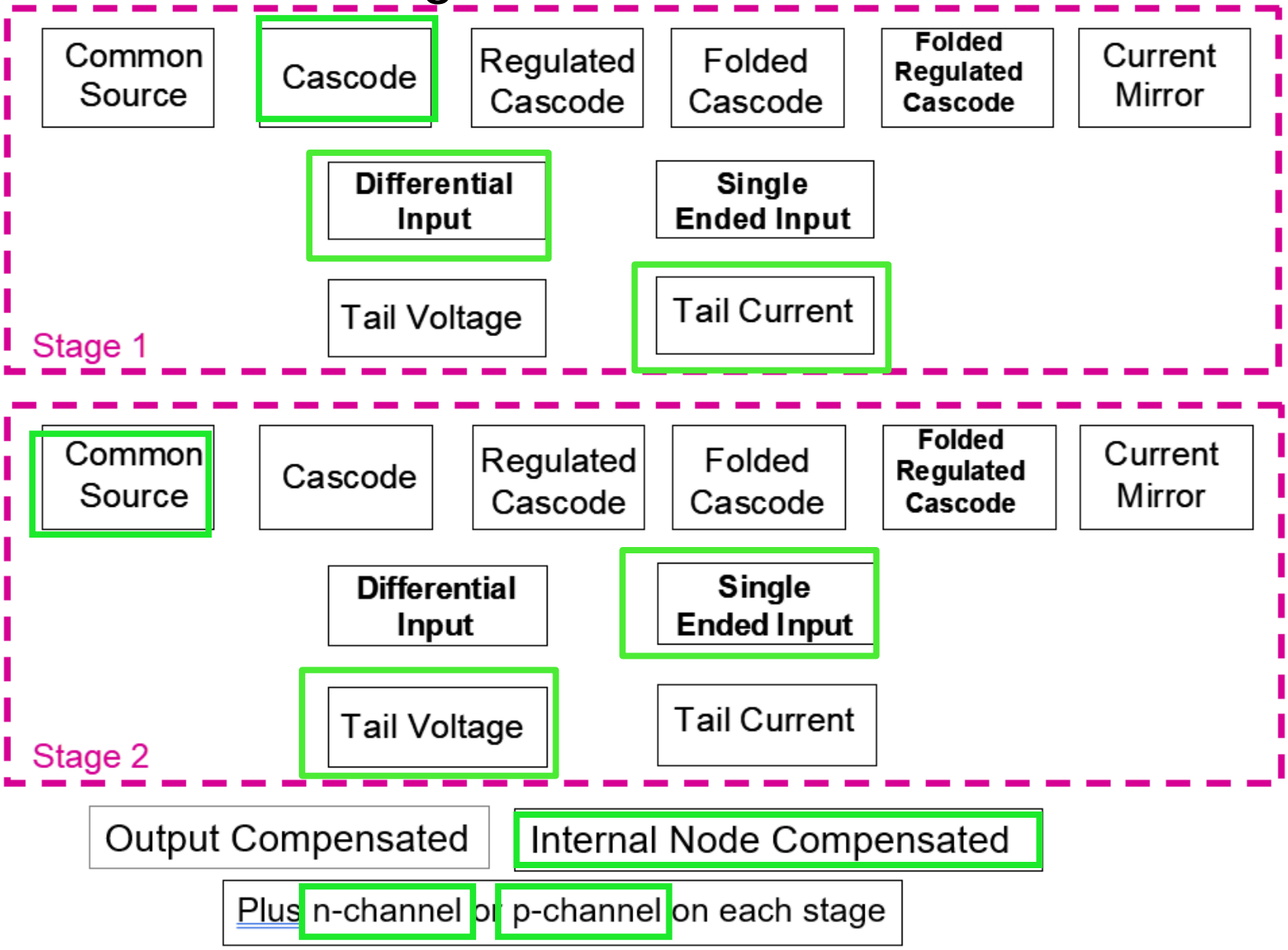
ADA4627-1/ADA4637-1 Data Sheet

Parameter	Symbol	Test Conditions/Comments	B Grade Min	B Grade Typ	B Grade Max	A Grade Min	A Grade Typ	A Grade Max	Unit
Settling Time to 0.01%	t_S								
ADA4627-1		V_{IN} = 10 V step, C_L = 35 pF, R_L = +1 kΩ, A_V = −1		550			550		ns
ADA4637-1		V_{IN} = 10 V step, C_L = 35 pF, R_L = +1 kΩ, A_V = −4		300			300		ns
Settling Time to 0.1%	t_S								
ADA4627-1		V_{IN} = 10 V step, C_L = 35 pF, R_L = +1 kΩ, A_V = −1		450			450		ns
ADA4637-1		V_{OUT} = 10 V step, C_L = 35 pF, R_L = +1 kΩ, A_V = −4		200			200		ns
Gain Bandwidth Product	GBP								
ADA4627-1		R_L = 1 kΩ, C_L = 20 pF, A_V = 1	16[4]	19		16[4]	19		MHz
ADA4637-1		A_V = 10		79.9			79.9		
Phase Margin	Φ_M								
ADA4627-1		R_L = 1 kΩ, C_L = 20 pF, A_V = 1		72			72		Degrees
ADA4637-1		A_V = 10		85			85		
Total Harmonic Distortion + Noise	THD + N	V_{IN} = 6 V rms, f = 1 kHz, A_V = 1, ADA4627-1		0.000045			0.000045		%

Example:

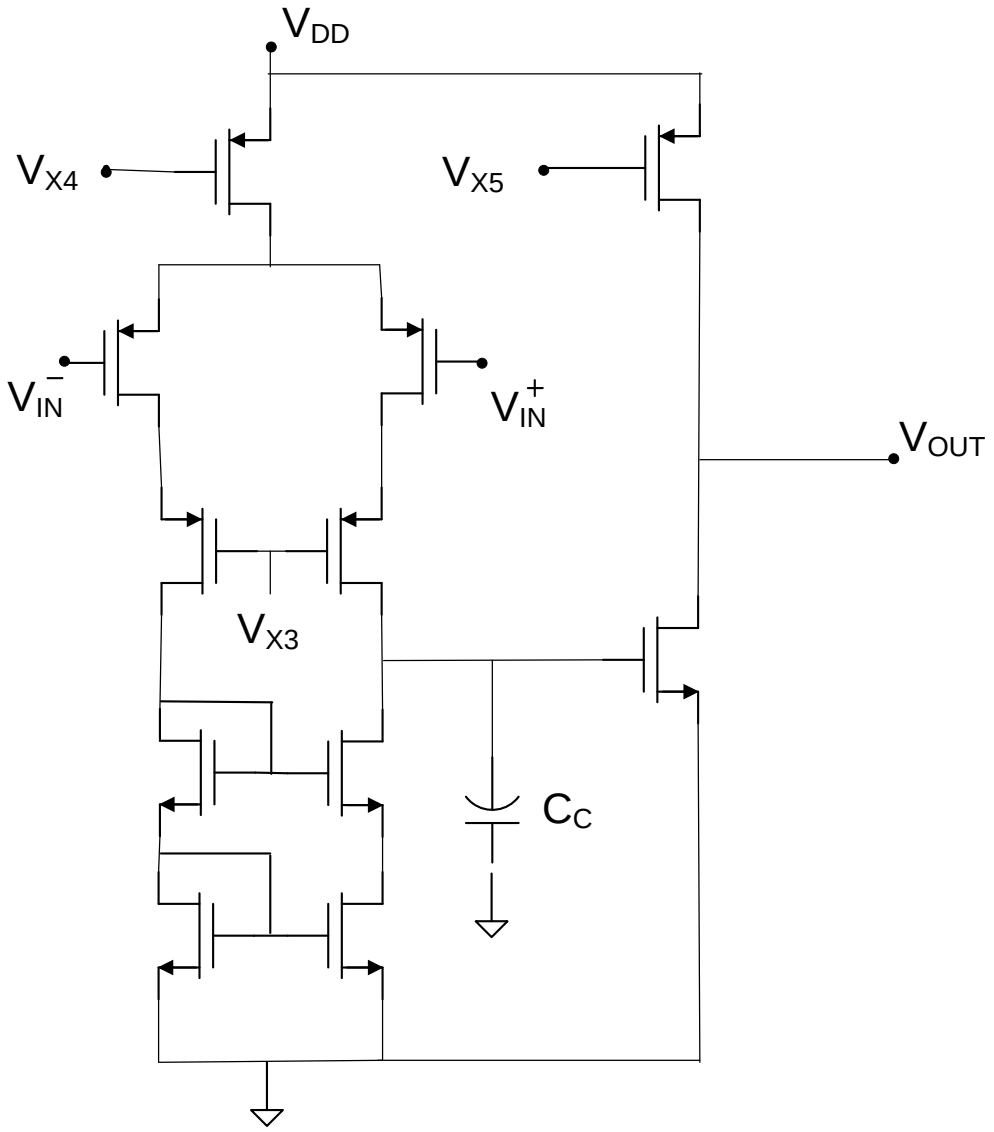
Sketch the circuit of a two-stage internally compensated op amp with a telescopic cascode first stage, single-ended output, tail current bias first stage, tail voltage bias second stage, p-channel inputs and n-channel inputs on the second stage.

Two-stage Architectural Choices



Cascode-Cascade Two-Stage Op Amp

Example Solution



First Commercial Operational Amplifier

K2-W Op Amp by Philbrickk, 1952-1971

Inventor of the Two-Stage Op Amp

Robert Widlar

Many say he started the field of analog IC design, considered a brilliant engineer

"Widlar began his career at Fairchild semiconductor, where he designed a couple of pioneering op amps. By 1966, the commercial success of his designs became apparent, and Widlar asked for a raise. He was turned down, and jumped ship to the fledgling National Semiconductor. At National he continued to turn out amazing designs, and was able to retire just before his 30th birthday in 1970."

(from posted www site)

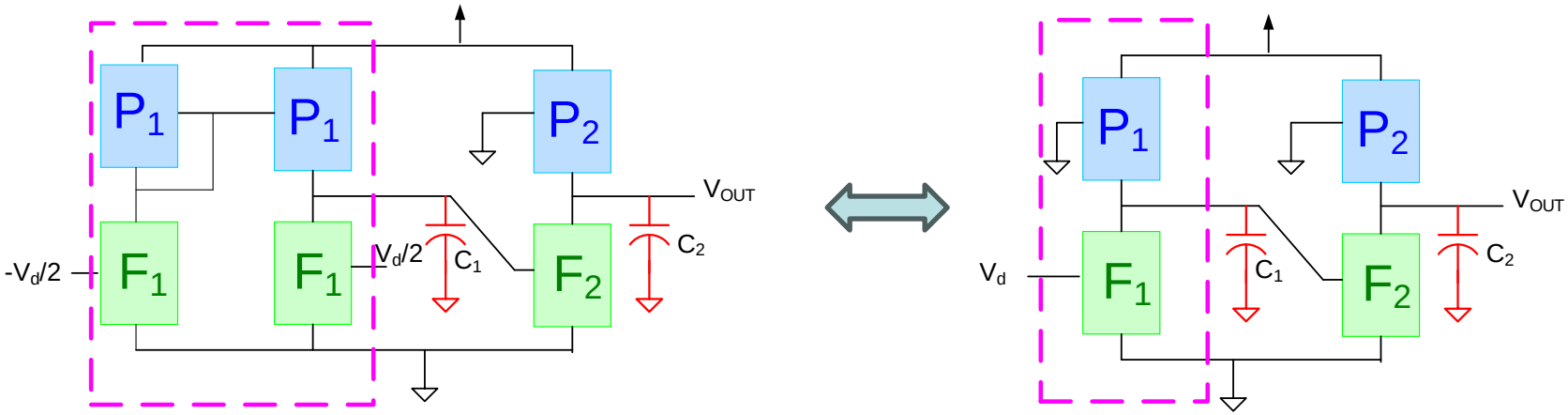
Inventor of the internally-compensated Op Amp

Dave Fullagar

(from posted www site)

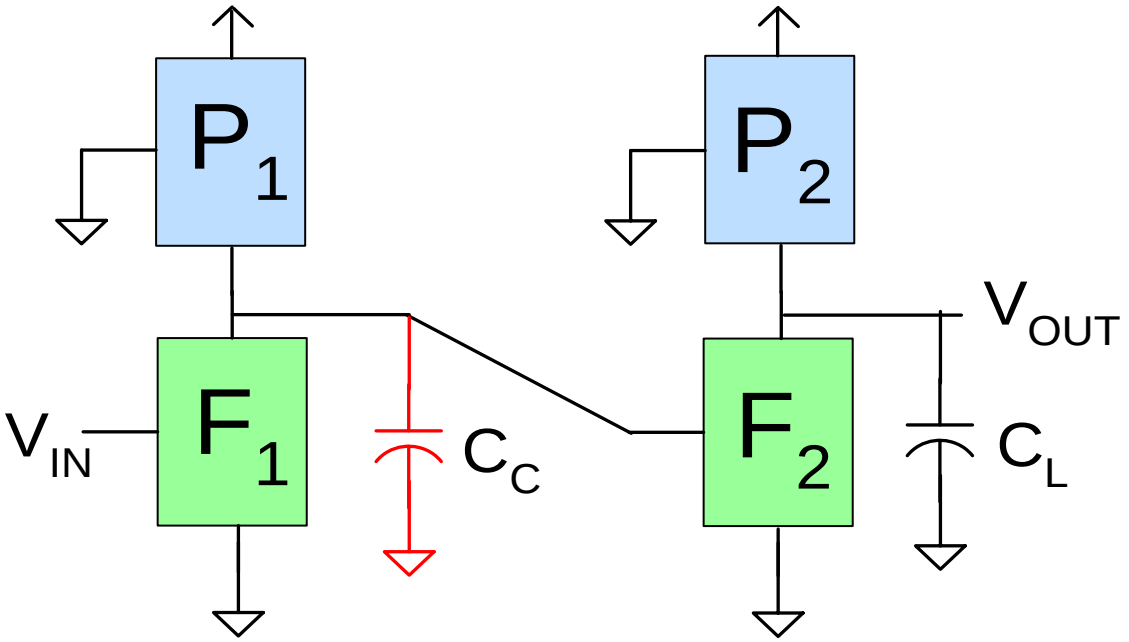
- Designed the first internally-compensated (C_C on chip) op amp, the 741
- Fullagar was 26 years old when this was designed (introduced?)
- Introduced in 1968
- Largest selling integrated circuit ever
- Still in high-volume production even though over 50 years old
- Fullagar later started the linear design activities at Intersil
- Cofounder (catalyst) of Maxim

Analysis of Internal-Node Compensated Two-Stage Op Amps



It can be shown that the small-signal differential analysis and the single-ended analysis of these two circuits give the same results

Analysis of Internal-Node Compensated Two-Stage Op Amps



p_1 pole on first stage, p_2 pole on second stage

(don't confuse **P_1** and **P_2** which is a symbols for counterpart circuit with poles p_1 and p_2)

Consider single-ended input-output (differential analysis gives same results)

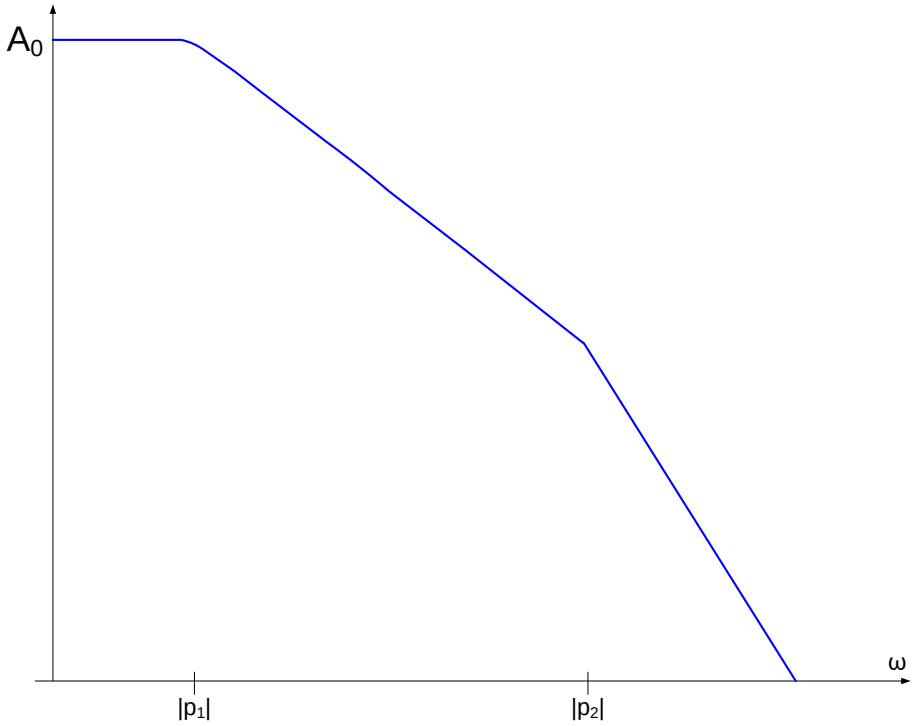
Can't get everything but can get most of the small-signal results

Since internal node compensated, must have $p_1 << p_2$

Analysis of Internal-Node Compensated Two-Stage Op Amps

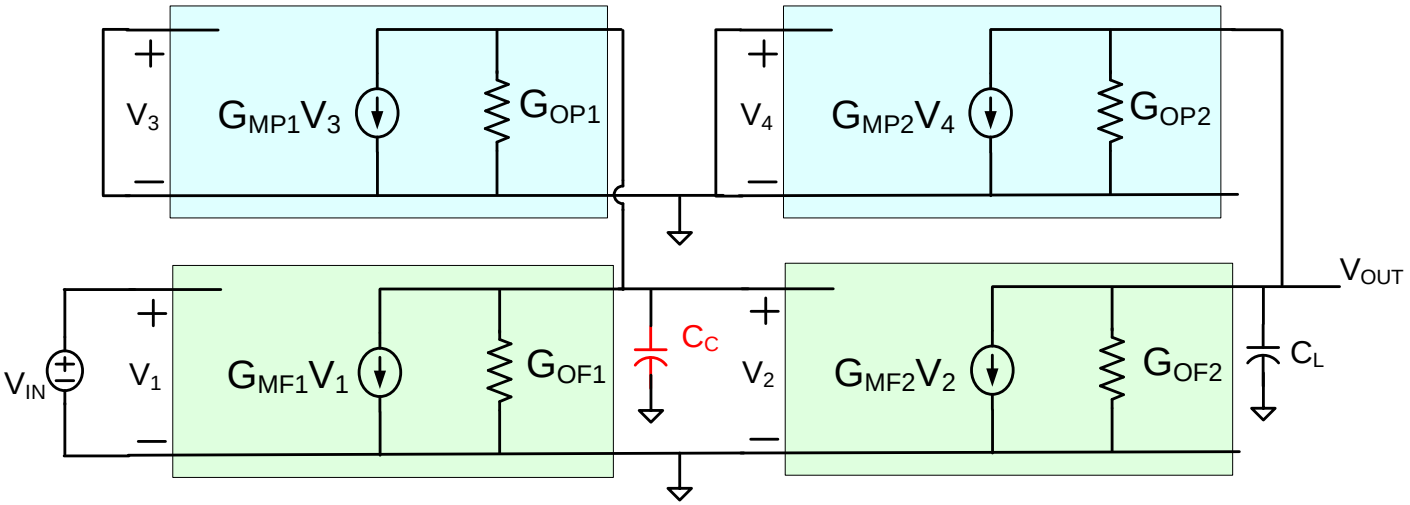
$$A(s) = \frac{A_0}{\left(\frac{s}{|p_1|}+1\right)\left(\frac{s}{|p_2|}+1\right)}$$

For $|p_1| << |p_2|$



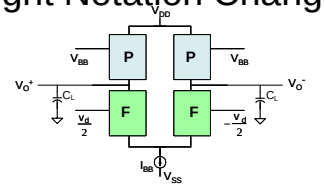
$BW \approx |p_1|$

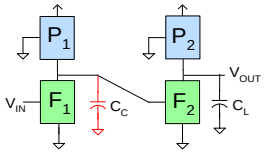
Analysis of Internal-Node Compensated Two-Stage Op Amps

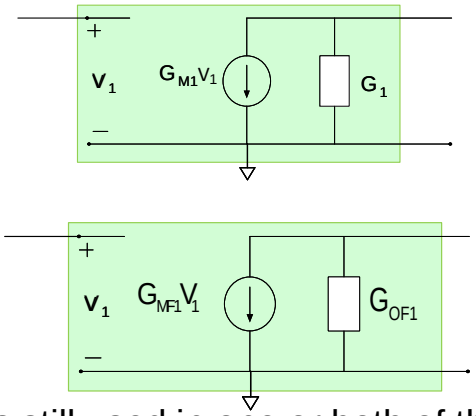


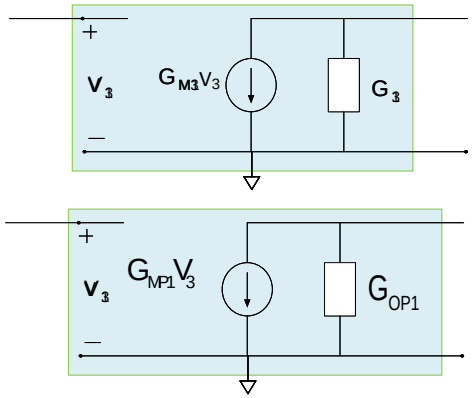
General Two-Stage Formulation

Slight Notation Change from what was used for Single-Stage Symmetric to Two-Stage Structures:



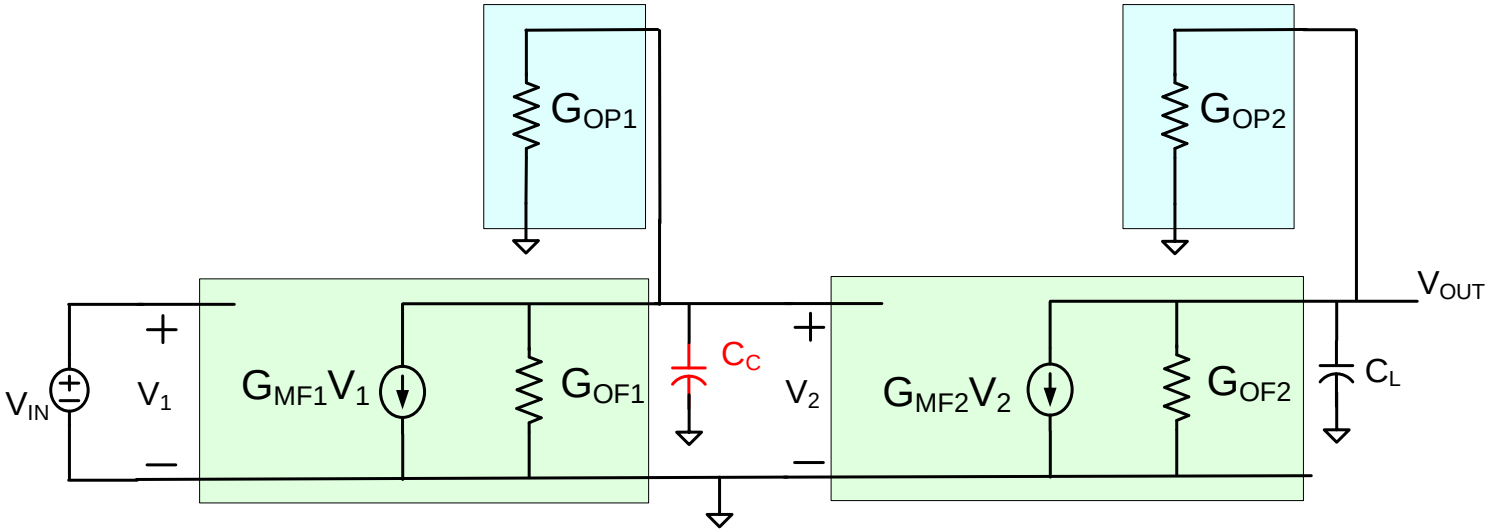






Symmetry on one or both stages still used in one or both of the two-stage amplifiers but not depicted here

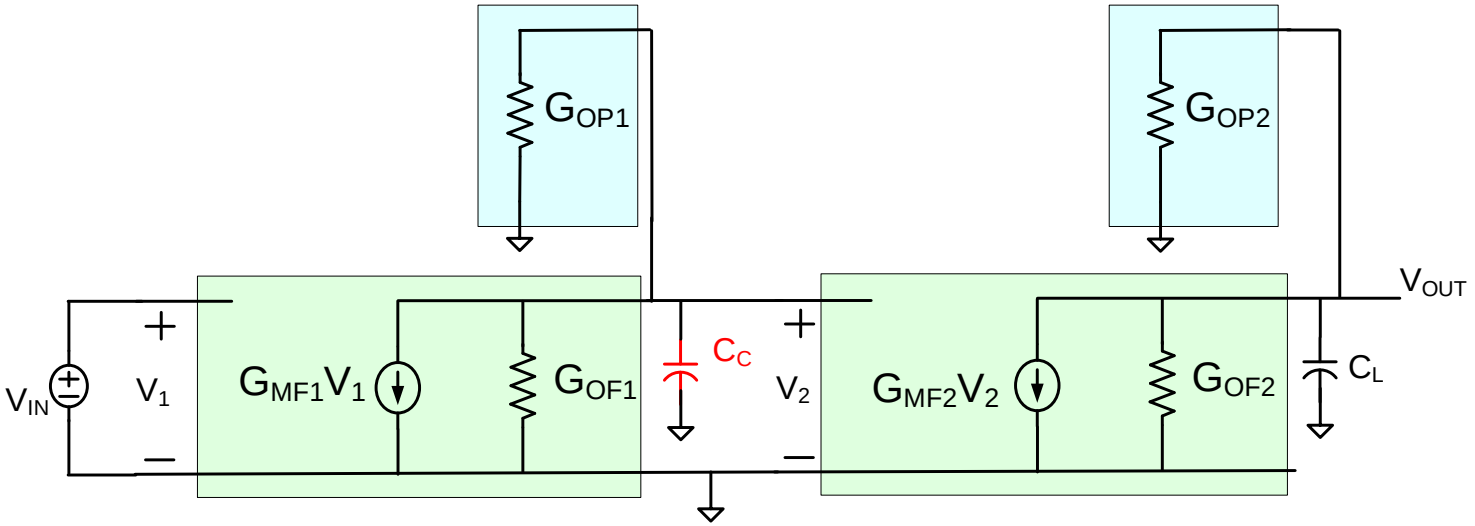
Analysis of Internal-Node Compensated Two-Stage Op Amps



$$\left.\begin{aligned} V_2\left(sC_C + G_{OF1} + G_{OP1}\right) + G_{mF1}V_{IN} &= 0 \\ V_{OUT}\left(sC_L + G_{OP2} + G_{OF2}\right) + G_{mF2}V_2 &= 0 \end{aligned}\right\}$$

$$A_V(s) = \frac{-G_{mF1}}{sC_C + G_{OF1} + G_{OP1}} \bullet \frac{-G_{mF2}}{sC_L + G_{OP2} + G_{OF2}}$$

Analysis of Internal-Node Compensated Two-Stage Op Amps



$$A_{V0} = \left(\frac{G_{mF1}}{G_{oF1} + G_{OP1}}\right)\left(\frac{G_{mF2}}{G_{OF2} + G_{OP2}}\right)$$

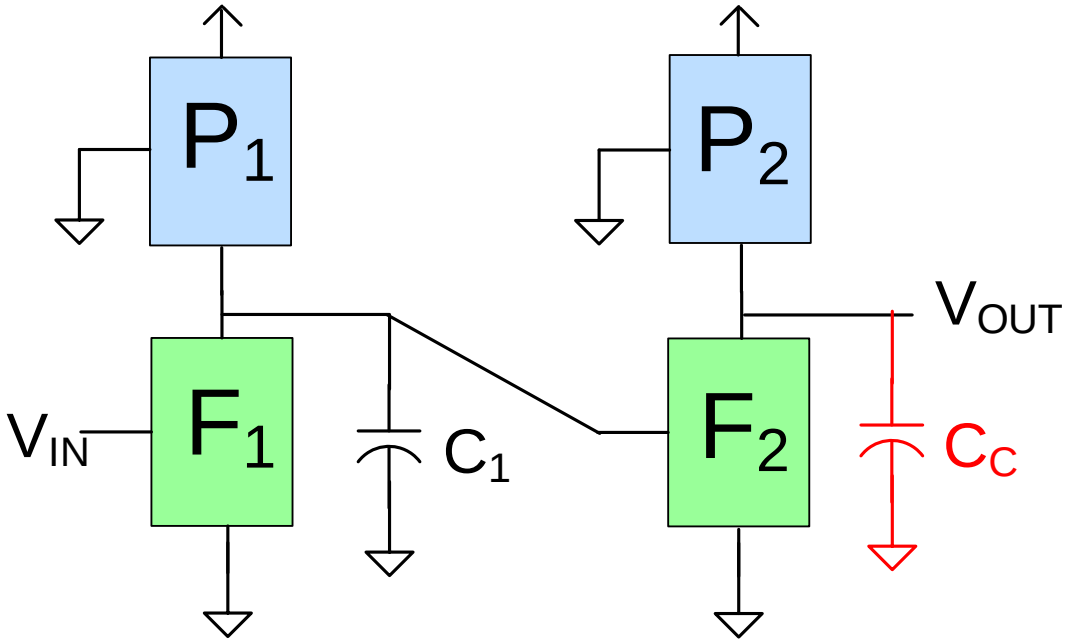
$$|p_2| = \frac{(G_{OF2} + G_{OP2})}{C_L}$$

$$|p_1| = \frac{(G_{OF1} + G_{OP1})}{C_C}$$

$$\mathbf{BW} = |\mathbf{p_1}|$$

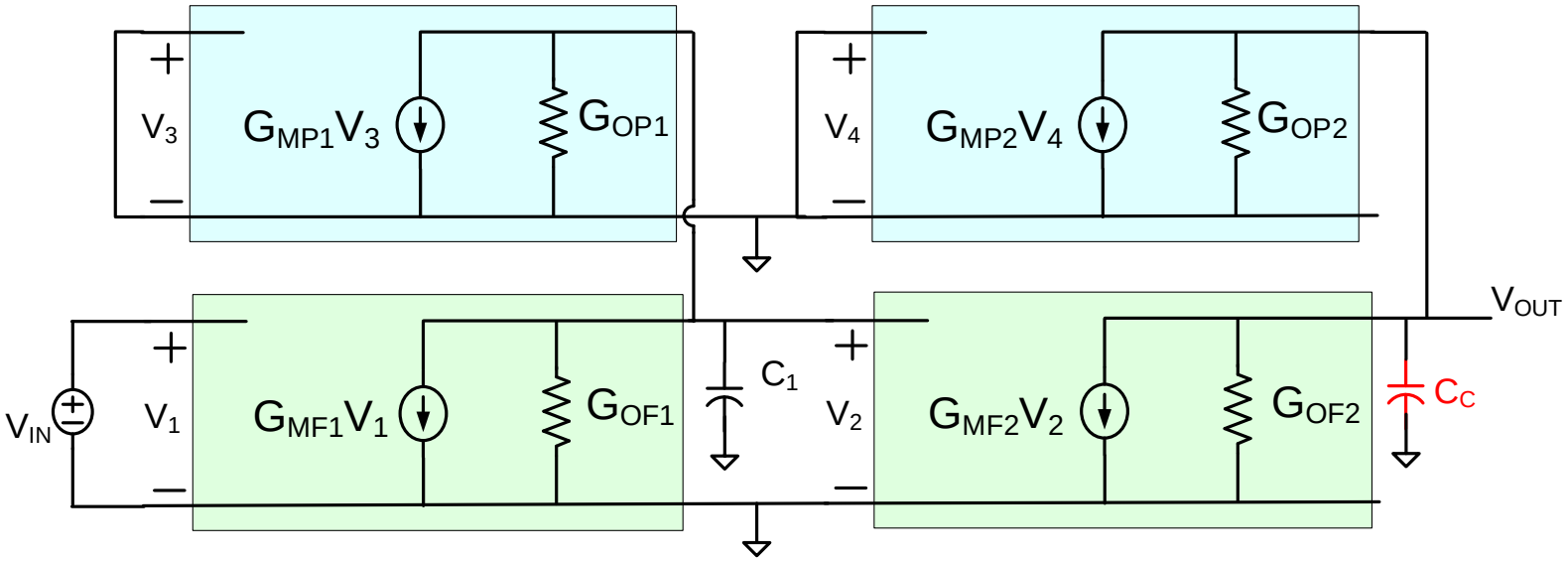
$$GB = \frac{G_{mF1}G_{mF2}}{(G_{OF2} + G_{OP2})C_C}$$

Analysis of Load Compensated Two-Stage Op Amps

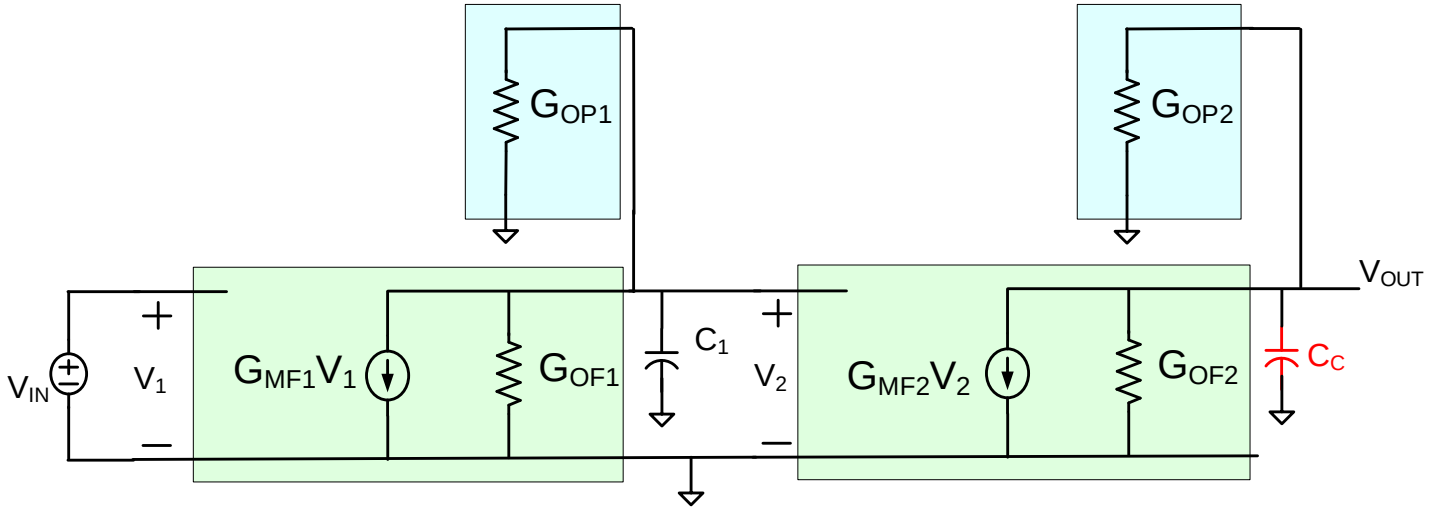


Can’t get everything but can get most of the small-signal results

Analysis of Load Compensated Two-Stage Op Amps



Analysis of Externally Compensated Two-Stage Op Amps



$$A_{V0} = \left(\frac{G_{mF1}}{G_{OF1} + G_{OP1}}\right)\left(\frac{G_{mF2}}{G_{OF2} + G_{OP2}}\right)$$

$$|p_2| = \frac{(G_{OF2} + G_{OP2})}{C_C}$$

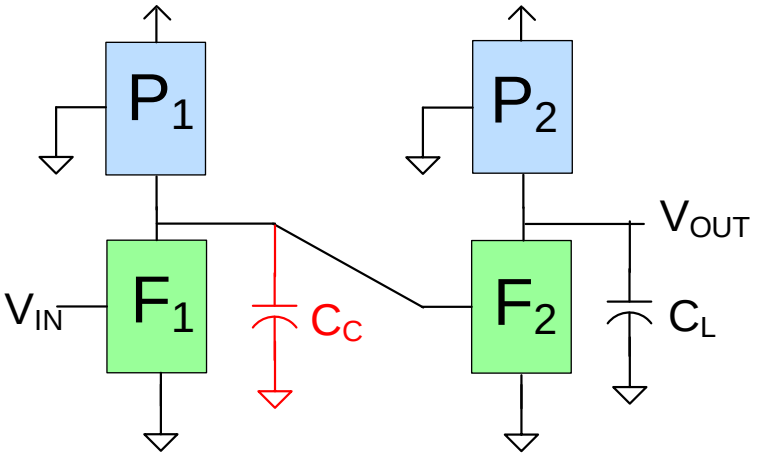
$$\mathbf{BW} = |\mathbf{p_2}|$$

$$|p_1| = \frac{(G_{OF1} + G_{OP1})}{C_1}$$

$$GB = \frac{G_{mF1}G_{mF2}}{(G_{OF1} + G_{OP1})C_C}$$

Determination of C_C

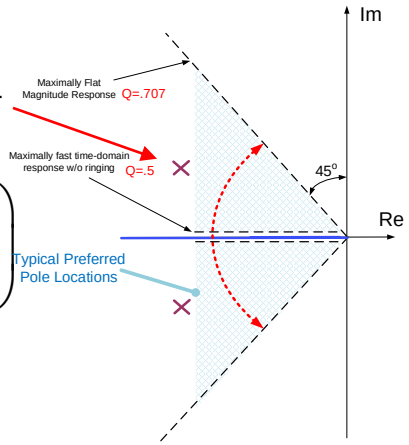
Consider Again the Internal-Node Compensated Two-Stage Op Amp



Recall approximate compensation requirements: $\mathbf{4\beta\, A_{0TOT} > k > 2\beta\, A_{0TOT}}$

where $|\mathbf{p_2}| = \mathbf{k}|\mathbf{p_1}|$

Thus, approximately, $\mathbf{3\beta\, A_{0TOT}} = \dfrac{|\mathbf{p_2}|}{|\mathbf{p_1}|}$ $\quad k \cong 3\beta\ A_{0TOT}$



$$3\beta\left(\frac{G_{mF1}}{G_{OF1}+G_{OP1}}\right)\left(\frac{G_{mF2}}{G_{OF2}+G_{OP2}}\right)\approx\left(\frac{G_{OF2}+G_{OP2}}{C_L}\right)\left(\frac{C_C}{G_{OF1}+G_{OP1}}\right)$$

$$C_C \approx \left(3\beta\frac{G_{mF1}G_{mF2}}{\left(G_{OF2}+G_{OP2}\right)^2}\right)C_L$$

Since the pole ratio needs to be very large, C_C gets very large !

Almost identical approach can be used to determine C_C for output compensation

Stay Safe and Stay Healthy !

End of Lecture 14